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graph TD
    MS20[Multimedia Source Memory 20]
    T30[Tuner 30]
    FE40[Feature Extraction Circuitry 40]
    A80[Analyzer Circuitry 80]
    MP90[Multimedia Processor 90]
    CPU10[Central Processing Unit CPU 10]
    M15[Memory 15]

    T30 --> FE40
    FE40 --> A80
    A80 --> MP90
    MS20 --> FE40
    MS20 --> MP90
    MP90 --> CPU10
    CPU10 --> M15
    M15 --> CPU10
    CPU10 -.-> T30
    CPU10 -.-> FE40
    CPU10 -.-> A80
    CPU10 -.-> MP90
```

The diagram illustrates a multimedia processing system architecture. On the left, a large block labeled "Multimedia Source Memory" (20) provides input to the "Feature Extraction Circuitry" (40) and the "Multimedia Processor" (90). The "Tuner" (30) is connected to the "Feature Extraction Circuitry" (40). The "Feature Extraction Circuitry" (40) feeds into the "Analyzer Circuitry" (80), which in turn feeds into the "Multimedia Processor" (90). The "Multimedia Processor" (90) outputs to the "Central Processing Unit (CPU)" (10). The "Central Processing Unit (CPU)" (10) is connected to "Memory" (15). Dashed lines indicate control signals between the CPU and the Tuner, Feature Extraction Circuitry, Analyzer Circuitry, and Multimedia Processor.

**Fig. 1**

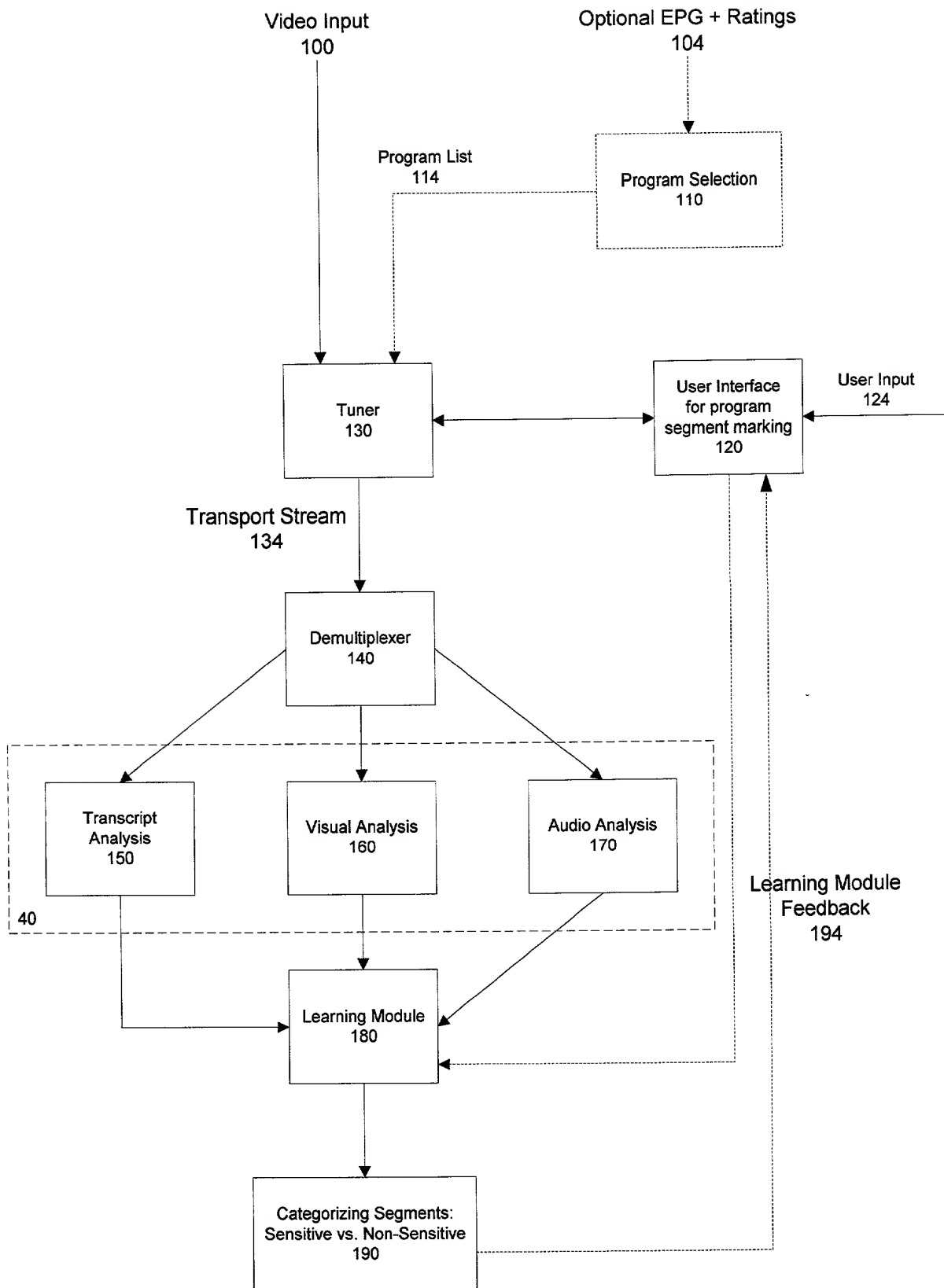


Fig. 2

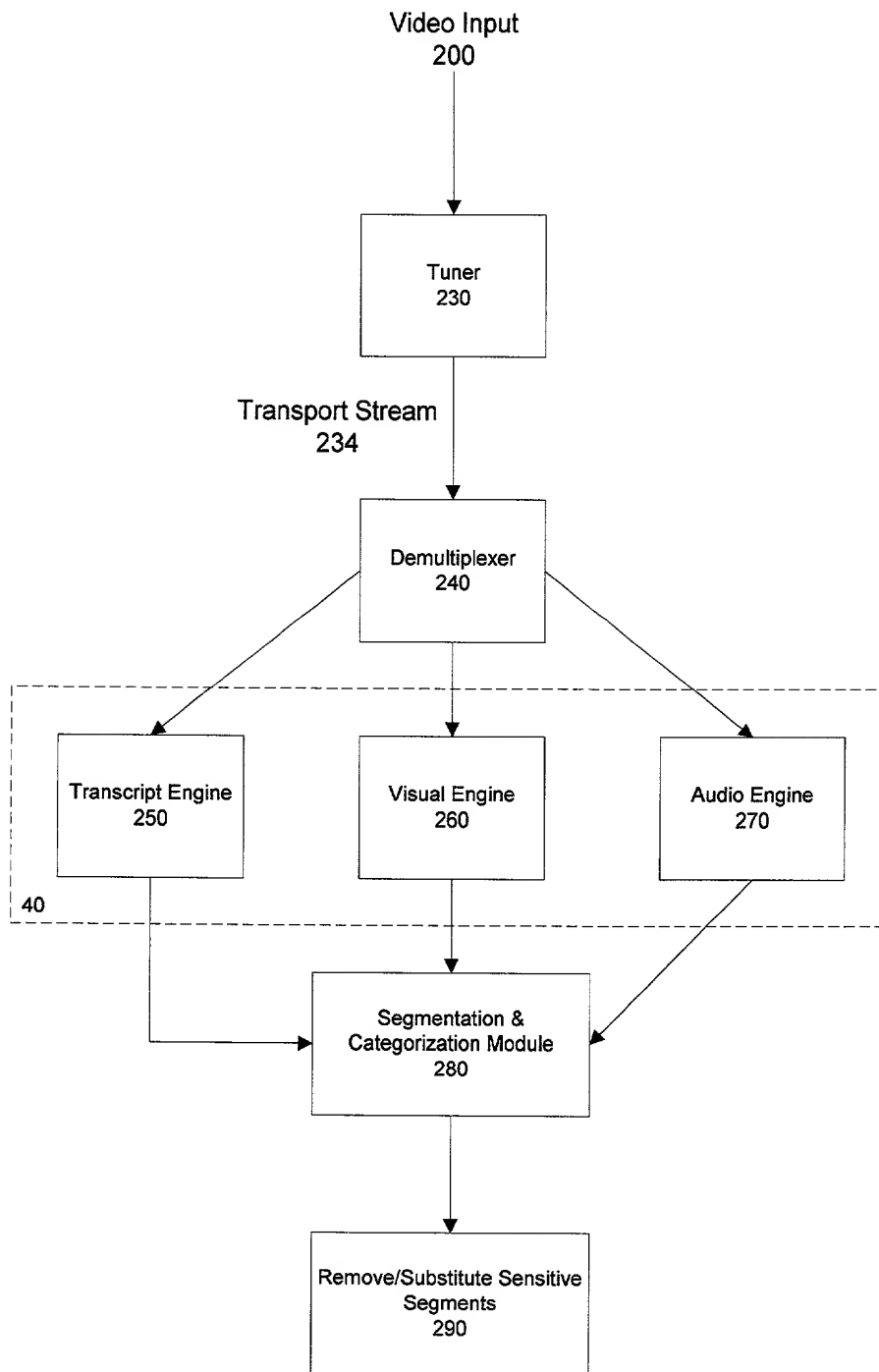


Fig. 3